



US006515987B1

(12) **United States Patent**  
**Carrozza et al.**

(10) Patent No.: **US 6,515,987 B1**  
(45) Date of Patent: **Feb. 4, 2003**

(54) **SERIAL TO PARALLEL CONVERSION OF DATA TO FACILITATE SHARING A SINGLE BUFFER AMONG MULTIPLE CHANNELS**

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\* cited by examiner

(75) Inventors: **Dominic P. Carrozza**, Redondo Beach, CA (US); **Gregory S. Caso**, Hermosa Beach, CA (US)

Primary Examiner—Ken Vanderpuye

(74) Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

(73) Assignee: **TRW Inc.**, Redondo Beach, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(57) **ABSTRACT**

The invention is a receiver and a method of receiving data having a preferred application in a satellite. A receiver in accordance with the invention includes at least one memory (118, 120), each memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal and outputs the stored data samples from a plurality of channels in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; and an outer decoder (102), responsive to data blocks with each data block containing at least one data group, which decodes the data blocks and outputs decoded data blocks.

(21) Appl. No.: **09/239,872**

(22) Filed: **Jan. 29, 1999**

(51) Int. Cl.<sup>7</sup> ..... **H04Q 11/04**

(52) U.S. Cl. .... **370/366; 370/316**

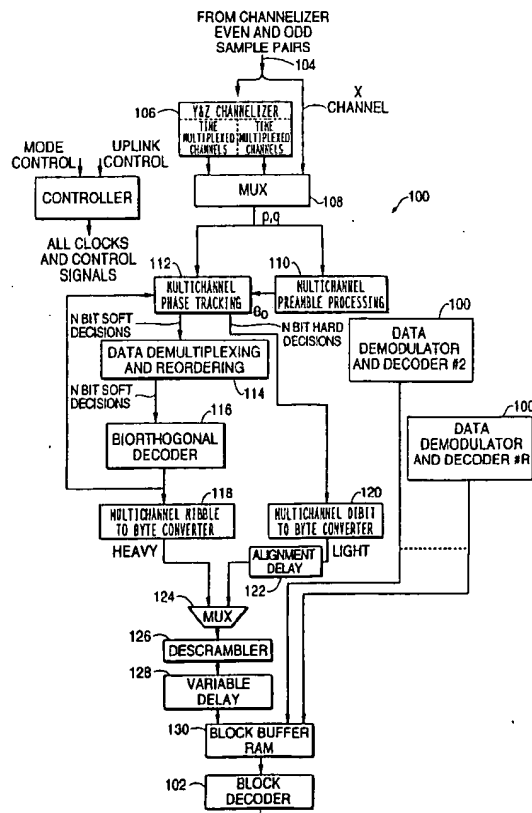
(58) Field of Search ..... 370/241, 242, 370/310.1, 314, 321, 337, 347, 442, 464, 366, 382; 714/746, 755, 756, 759, 760; 375/136, 137, 147, 316, 340, 341

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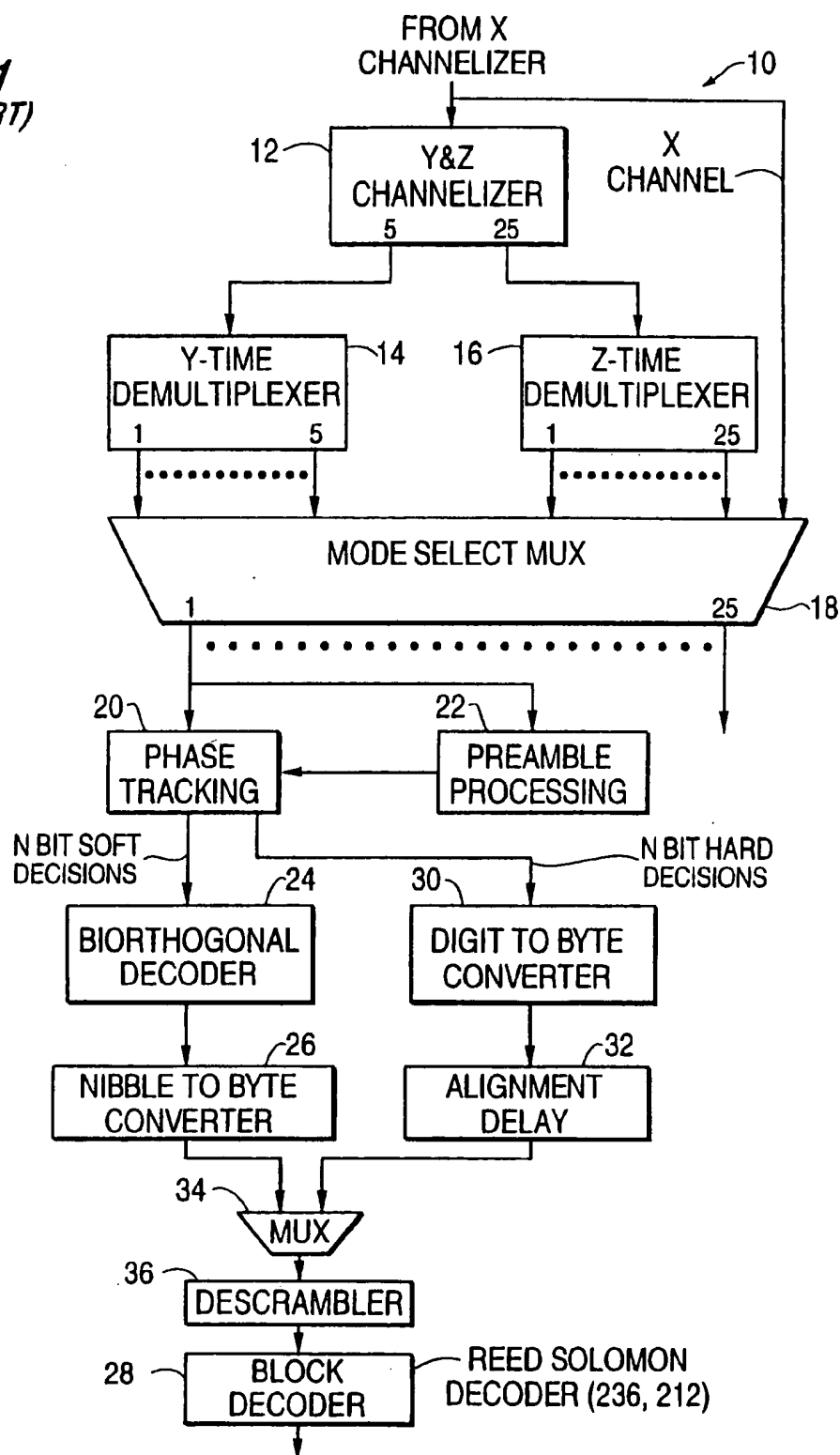
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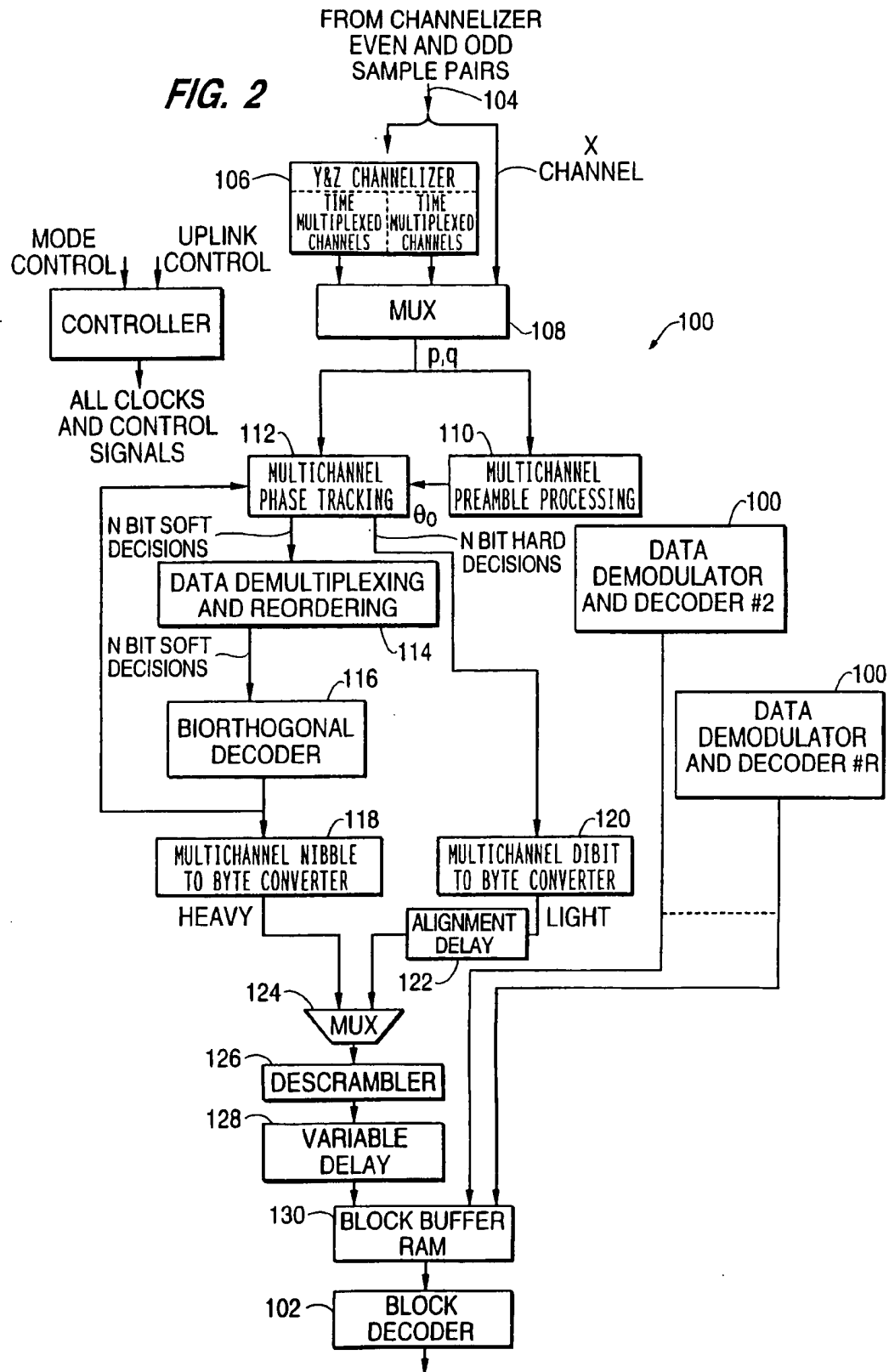
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**18 Claims, 4 Drawing Sheets**



**FIG. 1**  
(PRIOR ART)





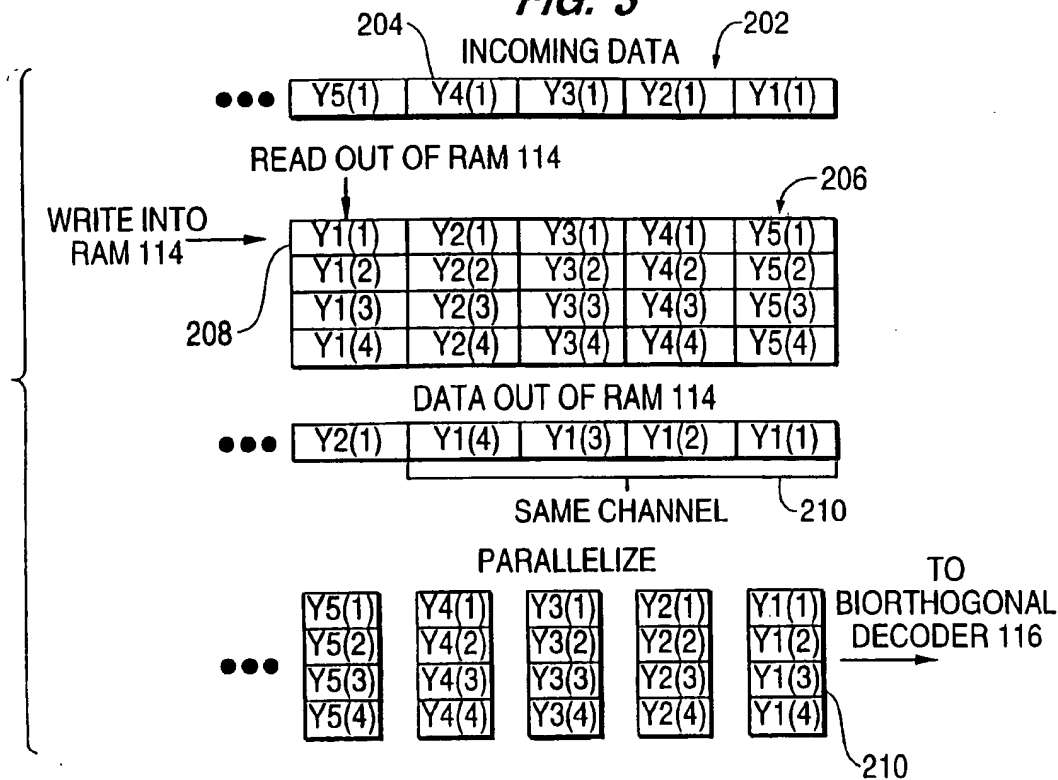
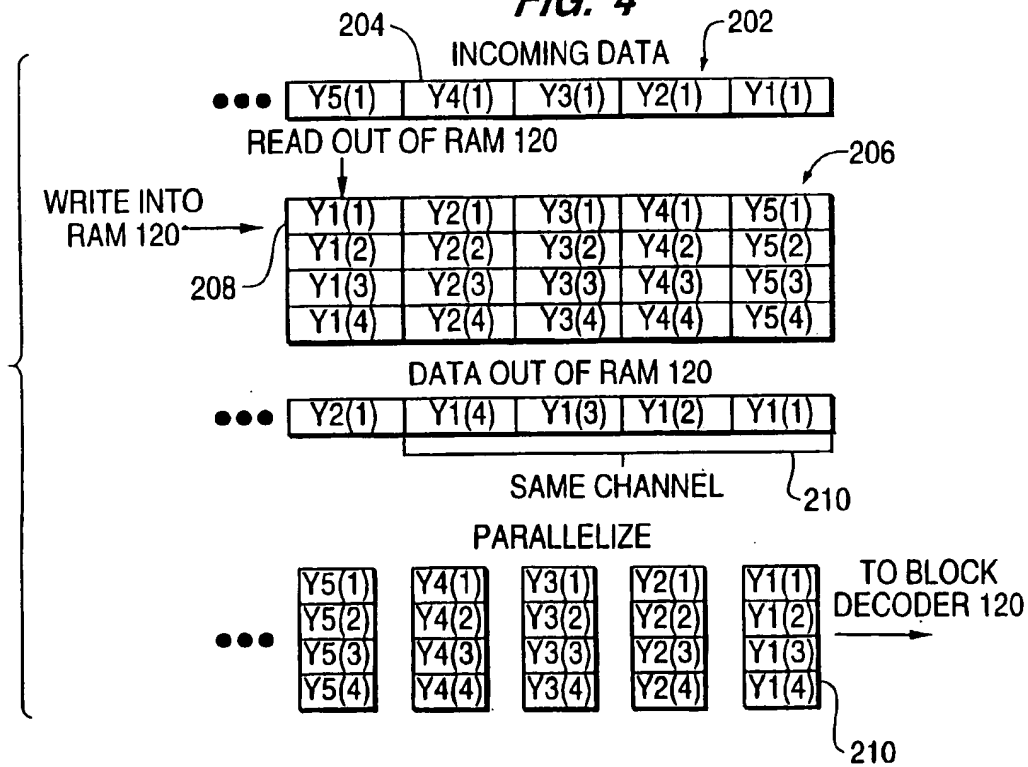
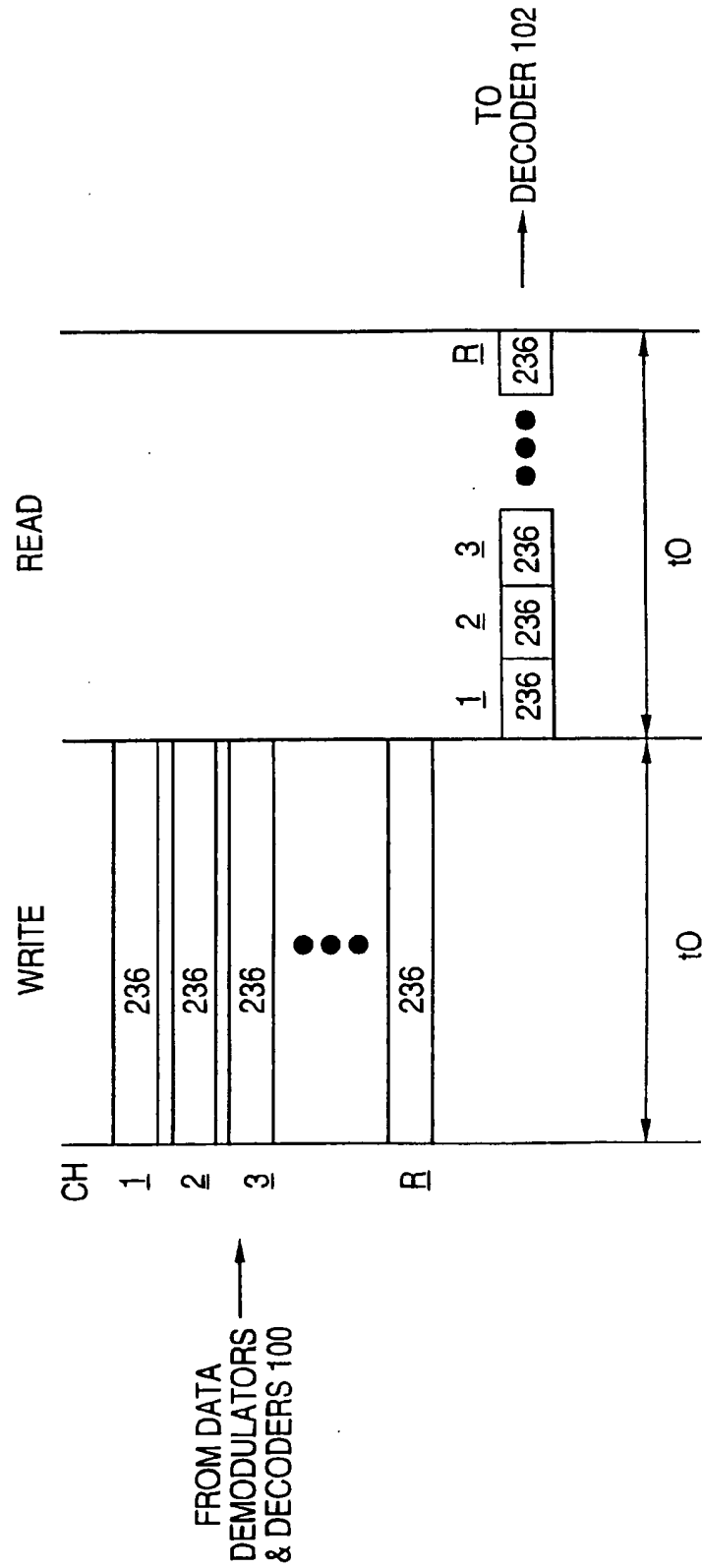
**FIG. 3****FIG. 4**

FIG. 5



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# SERIAL TO PARALLEL CONVERSION OF DATA TO FACILITATE SHARING A SINGLE BUFFER AMONG MULTIPLE CHANNELS

## CROSS REFERENCE TO RELATED APPLICATIONS

Reference is made to related applications entitled "Buffering and Sequencing of Soft Decisions of Multiple Channels Into a Single Shared Biorthogonal Decoder", filed on even date herewith Ser. No. 09/239,871; and "Buffering and Sequencing of Data From Multiple Channels Through a Shared Decoder", filed on even date herewith Ser. No. 09/240,171, which applications are incorporated herein by reference in their entirety.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to data receivers and methods of data reception and more particularly to data receivers in satellites and methods of receiving data with satellites which have reduced hardware for demodulating and decoding of data.

### 2. Description of Prior Art

Channelizers are well known in satellite data reception and function to divide a wide band received signal into a plurality of narrower band signals each of equal bandwidth. The data transmitted on a satellite uplink is typically frequency division multiplexed (FDM) and is divided into sub-bands by channelizers. Depending on the application, the sub-bands are again divided into narrower channels by additional channelizers.

Transmission access is further divided by time division multiplexing (TDM) into slots occupied by a transmission burst. These bursts utilize phase shift keying (usually either BPSK or QPSK) as the modulation method. Typically the bursts have a header that facilitates forming an initial estimate of the carrier phase and a body which carries information typically decoded by means of an error correction code.

Certain functions must be performed to receive data by a satellite which are, separation of the various uplink channels by frequency; the recovery of estimates of the modulated data from the burst body and the passing of the estimates to error correction processing, and the performing of decoding. In some applications, the data content of the burst is encoded in the form of ATM cells which are well known. When encoding utilizes ATM cells, it is necessary to recover the cells from the decoded data and to perform integrity checks upon them.

A satellite data reception system typically has three major sub systems. First, the aforementioned channelizer partitions the frequency spectrum of a beam into sub-bands. A sub-band demodulator and decoder performs demodulation and inner decoding on the signal in each sub-band outputted by the channelizer. A block and cell level processor (block decoder) typically processes the output of each inner decoder to perform outer decoding and cell level functions.

Signals within a sub-band may be arranged into one of three configurations. The sub-band demodulator and inner decoder must have functional capability to process each configuration, which are Type Z where the sub-band signal is configured as twenty-five narrow bandwidth, low data rate channels sharing the bandwidth by FDM; Type Y which is configured for five medium bandwidth channels, again

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shared by FDM, and Type X which is configured for a single wide bandwidth, high data rate channel occupying the full bandwidth.

In each of the sub-band FDM modes discussed above, transmission may occur in one of two error correction modes which are, heavy or light. In both the heavy and light cases, an outer code is used for data encoding which is typically a Reed-Solomon code over GF (256) of size (236, 212). In the heavy case, an inner code is also used. This inner code is typically a short rate one-half block code as, for example, the (8,4) biorthogonal code.

Jointly, there are six possible modes of data transmission, which are, XH, XL, YH, YL, ZH, and ZL. In each of these modes, the uplink transmission is organized time wise into frames typically of ninety-three milliseconds where each frame has two portions which are a synch burst portion and a traffic burst portion occupying three and ninety milliseconds respectively. The demodulator inner decoder and data decoder is not required to process the synch burst field. The traffic burst field consists of a number of slots within which individual traffic bursts may be placed by an uplinking earth terminal. Typically, the number of slots in ZH mode is twenty four and in ZL mode is forty eight. In YH and YL modes, there are typically five times as many slots per frame. In XH and XL modes, there are typically twenty five times as many slots per frame. The cumulative encoded data rate is the same in heavy and in light modes in each of the modes X, Y and Z and is typically 0.5, 2.5 and 12.5 megasymbols per second respectively. The demodulator and decoder is required to examine the signal present in each burst slot, demodulate it and decode it regardless of whether it contains a valid traffic burst which is assigned to the uplinking terminal. The demodulator and decoder is required to function reliably with a phase of the uplink signal that is unknown. However, the demodulator and decoder may rely on the signal amplitude being well controlled as a result of uplink power control methods and may rely upon the incoming frequency of both a symbol carrier and the symbol timing being closely aligned to the demodulator and decoder timing. Unlike other burst demodulators, the demodulator and decoder in a satellite relies on the time alignment of the bursts that it is required to process being very precise so that the demodulator and decoder does not need to provide burst continuous delineation for symbol time recovery functions.

Since the ATM protocol requires the cells to be delivered in the same order that they are presented and since usage may involve demultiplexing where more than one channel is used to transport a cell stream, the demodulator and decoder must be sure that all bursts are processed in a predictable order when channelization is used (modes Y and Z) and that burst time order is preserved when heavy and light coding modes are mixed across channels. When the X mode is used, only a single channel is present and all bursts are either in heavy or light mode.

Each of the R decoders and demodulators 10 of the prior art of FIG. 1 receives an input from an X channelizer which provides a sub-band of data which may be divided into five equally spaced Y mode channels or twenty five Z mode channels by a Y and Z channelizer 12. The Y and Z channelizer 12 outputs five channels to a Y time demultiplexer 14 and twenty five channels to a Z time demultiplexer 16.

The direct input from the X channelizer, the five output channels from the Y time demultiplexer and twenty five channels from the Z time demultiplexer are applied to a mode select multiplexer 18 which has a total of twenty five

output channels which are identically processed. Only the processing of the first output channel is described herein but it should be understood that the remaining twenty four channels are processed in the same manner with duplicated hardware and processing.

An output channel from the mode select multiplexer 18 is applied to a phase tracking function 20 and a preamble processing function 22 which function together as a phase estimation unit which correlates I and Q samples  $\{p(n)\}$  and  $\{q(n)\}$  against  $\{t(n)\}$  wherein  $\{t(n)\}$  is typically a M length sequence of + and -1's to produce variables I and Q as follows for light coding:

$$I = \text{SUM}[n=1 \text{ to } M: p(n) * t(n)] \quad Q = \text{SUM}[n=1 \text{ to } M: q(n) * t(n)]$$

The phase tracking for heavy burst repeats this operation and sums the two results. The phase tracking function then estimates the initial phase of the burst  $\theta_0$  by taking the arctangent of the ratio Q/I:

$$\theta_0 = \text{ATAN}[Q/I]$$

This correlation action is typically performed in a standard accumulator configured to add or subtract as required by the sign of  $t(n)$  and the phase estimate is typically produced using a ROM. The estimate  $\theta_0$  of the starting phase is supplied to the phase tracking function 20. The phase estimation provided by the combination of the phase tracking and aforementioned preamble processing functions 20 and 22 provides the estimate  $\theta$  of the received signal phase in order to provide best bit error rate (BER) performance.

The phase lock loop provided by the phase tracking and preamble processing functions 20 and 22 operates in one of two modes relative to a decision direction depending upon whether the decoder and demodulator 10 is operating in the ZL or ZH modes. For light code bursts, the phase lock loop processes the  $\{p(n)\}$ ,  $\{q(n)\}$  sample pairs for each symbol as independent and forms an error estimate for the phase lock loop filter. In a typical case in the light mode, the phase lock loop is a first order phase lock loop which simply accumulates  $k * \epsilon_n$  to yield the phase estimate  $\theta$  wherein  $\epsilon_n$  is the phase error estimate for each sample pair. Since synchronization for advanced satellites maintains the uplink frequency within a very tight tolerance which is typically no worse than  $\pm 500$  Hz or equivalently, 0.001 revolution per symbol epoch for the slowest transmission data rate typically 500 kilobits per second for the Z mode, a simple first order loop with a gain k in the range of  $1/16$  is adequate to track the phase. The demodulator and decoder may optionally use a lower loop gain when processing bursts from modes Y and X which have a higher symbol rate.

For heavy coded bursts, four consecutive symbols are related which represent a code word in an (8,4) biorthogonal code which is well known. In this case, the decision direction is based on decoded results from the inner decoder 24 which receives the N BIT SOFT DECISIONS output from the phase tracking function 20 containing eight possible bits and outputs the four most likely bits in a manner which is well known. The output of the inner decoder 24 is in the form of a four-bit nibble which is applied to a nibble to byte converter 26 which converts consecutive nibbles from a single channel outputted from the inner decoder 24 into bytes for subsequent processing by outer decoder 28 which may be a Reed-Solomon decoder of well-known construction. The N BIT HARD DECISIONS output from the phase tracking function 20, which is in dibit groups, is applied to a nibble to byte converter 30, which outputs bytes from a single channel for subsequent decoding by the outer decoder

28. The output of the nibble to byte converter 30 is applied to an alignment delay 32 which provides time compensation for the processing delay produced by the inner decoder 24 so that the respective bytes outputted from the soft and hard processing paths become time aligned. The outputs from the nibble to byte converter 26 and the alignment delay 32 are applied to a multiplexer 34 which selects bytes from the soft or the hard decision path for inputting to a descrambler 36 of conventional construction which uses a scrambling code to prevent crosstalk between adjacent beams. The outer decoder 28 typically decodes GF (256) of size (236, 212).

The overall operation of the demodulator and decoder 10 is under the control of the onboard satellite processor (not illustrated) and receives timing signals from the satellite's uplink timing system which are not described in detail herein in view of their being well known.

The channelizer 10 has its simplest operation in the mode X. In this circumstance, all requisite filtering is performed by the X channelizer which provides the input to the decoder and demodulator 10. In the Y and Z processing modes, the Y and Z channelizer 12 is further required to divide the sub-band output from the X channelizer into further smaller channels for processing as described above.

The processing architecture of each of the output channels from the mode select multiplexer 18 requires substantial hardware for all twenty five Z channels, and is an inefficient decoding architecture for time multiplexed X channel data streams. This architecture has less efficiency, high complexity, requires more circuitry and consumes substantial DC power which provides reduced processing flexibility for data reception, especially in environments such as satellites. This architecture further requires substantial memory for processing all of the output channels from the mode select multiplexer 18.

#### SUMMARY OF THE INVENTION

The present invention is a receiver and method of receiving data transmissions having a preferred application for reception of data by satellites. The invention buffers and sequences data from multiple channels at selected processing locations in a demodulator and decoder downstream of the output of the phase tracking function which reduces the number of nibble to byte converters, nibble to byte converters and block decoders compared to the prior art. As a result, increased data processing efficiency, better redundancy of processing, reduced consumption of DC power and miniaturization of circuitry is achieved while also providing greater processing flexibility.

A multichannel data demultiplexing and reordering memory processes the output data from multiple channels outputted from the phase tracking function. Time division multiplexed (TDM) processors of multiple channels eliminates parallel processing paths for each of the channels as in the prior art which required a soft and a hard decision processing path for each of the channels.

The invention further is a converter which combines inputs of one or more bits from multiple TDM channels outputted from the phase tracking function into multibit outputs for processing by a single outer decoder. As a result, the parallel processing of the prior art having individual inner decoders for each channel is eliminated. The converter is used in both the TDM multiple channel soft and hard decision processing paths which are outputted from the phase tracking function.

The invention further is a block memory which converts groups of bits from multiple TDM channels into blocks of

bits each containing at least one group of bits for sequential decoding by an outer decoder. The block memory eliminates the requirement of an outer decoder in each channel as in the prior art. Outer decoders have sufficient processing speed to sequentially demodulate each of the blocks stored in the block memory which are readout and decoded within the time in the prior art that a single block is decoded.

A receiver in accordance with the invention includes at least one memory, each memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal and outputs the stored data samples from a plurality of channels in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; and an outer decoder, responsive to data blocks with each data block containing at least one data group, which decodes the data blocks and outputs decoded data blocks. A pair of data processing paths is provided with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, the pair of data processing paths each containing one of the at least one memory. The soft decision processing path further comprises upstream of one of the at least one memory, another memory including an addressable storage array which stores a sequence of data samples contained in the time division multiplexed signal and outputs the stored data samples in a sequence of the data groups, each data group containing a plurality of samples from one of the plurality of channels and an inner decoder, responsive to the data groups, which decodes the data samples within the data groups and outputs the decoded data samples to the memory in the soft decision processing path. The data samples inputted to the another memory each comprise orthogonally encoded data; and the inner decoder is a biorthogonal decoder. The inner decoder is a Reed-Muller decoder. The receiver is contained in a satellite. The receiver further includes a channelizer, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the channels comprising the time division multiplexed signal. The memories each further comprise a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator. The another memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the another memory with addresses generated by the write address generator and the sequence of data groups outputted from a group of memory cells of the another memory with addresses generated by the read address generator.

A method of data reception in accordance with the invention includes storing in at least one memory a received time division multiplexed signal containing a sequence of data samples from a plurality of channels; from the at least one memory outputting the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; decoding with an outer decoder the data samples within data blocks with

each data block containing at least one data group; and outputting the decoded data samples of the plurality of data blocks. A pair of data processing paths are provided with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, and wherein each data processing path contains one of the at least one memory, each memory storing a received time division multiplexed signal containing a sequence of data samples from the plurality of channels, outputting from each memory the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels, decoding the data samples within the data blocks each containing at least one data group, and outputting the decoded data samples. The soft decision path contains another memory, upstream of the memory, which stores a sequence of the data samples and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; the data group is decoded with an inner decoder; and the data decoded by the inner decoder is outputted to the memory of the soft decision processing. The data samples inputted to the another memory each comprise orthogonally encoded data; and the inner code decoder is a biorthogonal data encoder. The method is performed within a satellite. An input bandwidth is divided with a channelizer into a plurality of output channels each having an equal bandwidth, one of the output channels comprising the time division multiplexed signal. Memory cells of each of the at least one memory are addressed by addresses generated by a read address generator and a write address generator with the sequence of data samples being written in a data group of memory by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a block diagram representative of a prior art demodulator and decoder of a type used in a satellite.

FIG. 2 illustrates a block diagram of a demodulator and decoder in accordance with the present invention having a preferred application in a satellite.

FIG. 3 illustrates the operation of a multichannel data demultiplexing and reordering memory in accordance with the present invention.

FIG. 4 illustrates the operation of a multichannel data converter which converts one or more bits into output words of an increased number of bits in hard and soft decision paths in accordance with the present invention.

FIG. 5 illustrates the operation of a block buffer memory in accordance with the present invention which converts data outputs from multiple demodulators and decoders into a data structure for sequential demodulation by a single outer decoder.

Like reference numerals identify like parts throughout the drawings.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 2 illustrates a block diagram of a data demodulator and decoder 100 in accordance with the present invention. The data decoder and demodulator 100 differs from the prior art by processing multiple channel outputs from a phase



tracking function in each data demodulator and decoder 100. As illustrated, a plurality of channels, which are R in number, are decoded by a single outer decoder 102 as described below to sequentially process the parallel inputs from the R data demodulators and decoders 100 within a time interval used to process an output of a single data demodulator and decoder 10 in the prior art. An input 104 from an X channelizer is applied to a Y and Z channelizer 106 of well-known construction which respectively processes the TDM Y and Z channels in accordance with the prior art discussed above. The input 104 from the X channelizer along with the Y and Z TDM output channels produced by the Y and Z channelizer 106 are applied to a multiplexer 108 which outputs either the X channel, the Y time multiplexed channels or the Z time multiplexed channels to multichannel preamble processing 110 and multichannel phase tracking 112. The preamble processing and phase tracking functions 110 and 112 may be in accordance with the prior art principles of control to produce proper phase lock loop tracking. The phase tracking function 112 has a N BIT SOFT DECISIONS output and a N BIT HARD DECISIONS output. The processing of the N BIT SOFT DECISIONS and the N BIT HARD DECISIONS is in accordance with the prior art except that multiple channels are processed with a multiple channel data demultiplexing and reordering memory 114, a multiple channel nibble to byte converter 118, a multiple channel dibit to byte converter 120, and block buffer 130 as described below.

The output from the phase tracking 112 of the N BIT SOFT DECISIONS is applied to a data multiplexing and recording memory 114, which may be a RAM or other type of memory, that functions to convert time multiplexed outputs from multiple channels into outputted sequences of bit groups from the individual channels as described below in conjunction with FIG. 3. The data multiplexing and reordering memory 114 includes an addressable storage array which stores a sequence of data samples contained in a TDM signal which is outputted from the multichannel phase tracking function 112 from a plurality of channels contained in the output 104 from the X channelizer. A write address generator and a read address generator are contained in the data demultiplexing and reordering memory 114 to respectively control generation of addresses which control writing of the TDM samples from multiple channels into the memory and the reading out of a sequence of data groups from the memory with each data group containing a plurality of samples from one of the plurality of channels as discussed below in conjunction with FIG. 3.

FIG. 3 illustrates the operation of the multiple channel data demultiplexing and reordering memory 114 which may be a RAM. The data is in accordance with a key of  $Y_m(n)$  wherein m is the channel number and n is the time index. Therefore, it is seen, for example, that the sample  $Y_1(1)$  is a data sample from channel number one at time index one. As illustrated, the "INCOMING DATA" 202 is TDM samples 204 from channels Y1, Y2, Y3, Y4 and Y5. Each sample 204 is representative of two-bit symbols which are encoded by QPSK encoding and each are stored in a pair of memory cells. The data structure after storing the sequence of individual lines 202 of "INCOMING DATA" is in the block 206 located to the right of the legend "WRITE INTO RAM". The block 206 is comprised of four rows 208 of data samples which are identical to the incoming data 202 and are sequentially read in columns from successive stored lines 202 of the block 206 of the stored TDM input data.

Each of the memory cells is in an addressable storage array addressed by the aforementioned write and read

addresses generated by write and read address generators contained in the memory in accordance with well-known memory addressing techniques. Each sequence of data samples in a line 202 of incoming data are written in a group of memory cells with write addresses spanning a full row 208. The bracket labelled "SAME CHANNEL" in the line labelled "DATA OUT OF RAM" identifies the continuous data samples of a single channel which are read out as a group 210. Finally, under the heading "PARALLELIZED" the read out of sequential data groups 210 is illustrated which are individually outputted from a group of memory cells of the memory addressed by read addresses the memory cells. It should be understood that the function of the data demultiplexing and reordering memory 114 is not limited to the processing of any number of bits.

The data groups 210 are inputted to a conventional inner decoder 116 which may be a biorthogonal decoder which performs the same function as the prior art inner decoder of FIG. 1 in outputting the most likely four bits within the eight bit input. The output of the inner decoder 116 is fed back to the multichannel phase tracking 116 to provide a more accurate phase error estimate  $\epsilon$  in the phase lock loop. In view of multiple channels of TDM data 202 being reordered into sequential groups of data 210 from individual channels by the data demultiplexing and reordering function 114, only a single inner decoder 116 is required to decode the inner code (e.g. 8,4 biorthogonal block code) from multiple channels instead of decoding only a single channel as in the prior art of FIG. 1.

A pair of multiple channel data converters 118 and 120 of similar construction respectively process the multiple bit outputs from the inner decoder 116 and from the data demultiplexing and reordering memory 114 to output words having a word length from one channel which the outer decoder 102 is designed to decode. The difference in the processing between the multiple channel nibble to byte converter 118 and the dibit to byte converter 120 is that the number of TDM input bits to the nibble to byte converter is four and the number of TDM input bits to the dibit byte converter is two with both converters producing a byte output. It should be understood that the processing performed by the converters 118 and 120 is not limited by any number of bits. The converters 118 and 120 convert data of multiple channels into larger data groups which are sized to facilitate efficient decoding by the outer decoder 102 which decodes data from a single channel during each decoding cycle. As a result, the number of converters required to process data with the present invention is reduced by a factor of the number of TDM channels in the data stream outputted by the phase tracking function 112.

Operation of the dibit to byte converter 120 is illustrated in FIG. 4 and is analogous to the operation of the data demultiplexing and reordering memory 114 illustrated in FIG. 3 described above in that two bit TDM samples are processed into a byte from one channel. The converter 120 also contains write and read address generators which address the writing and reading of data in the same manner as the data demultiplexing and reordering 114. The operation of the converter 120 is not repeated herein in view of its similarity to the operation of the demultiplexing and reordering memory 114 discussed above.

Furthermore, while not illustrated, operation of the nibble to byte converter 118 is analogous to the dibit to byte converter 120 except that only two TDM nibbles from multiple channels are inputted and one byte per channel is outputted to the block decoder 102. It should be understood that the processing performed by the converters 118 and 120 is not limited by any number of bits.

The converters 118 and 120 permit the conversion of TDM data from multiple channels into data groups which are sized for the decoding performed by the outer decoder 102. As a result, the number of converters required to process data with the present invention is reduced by a factor of the number of TDM channels which are in the data stream outputted by the phase tracking function 112.

The output of the dibit to byte converter 120 is applied to an alignment delay 122 which time aligns the N BIT SOFT and N BIT HARD DECISIONS inputted to a multiplexer 124 which selects one of the outputs from the nibble to byte converter 118 or dibit to byte converter 120 depending upon whether operation is in the heavy or light mode as described in the prior art above. The output of the multiplexer 124 is applied to a descrambler 126 which is in accordance with the prior art. The output of the descrambler 126 is applied to a variable delay 128 which provides time alignment between the outputs of the R data demodulator and decoders 100 which are inputted to a block buffer memory 130 which is coupled to a plurality of data channels respectively outputted from each of the data demodulators and decoders 100.

The block buffer memory 130 stores the inputted data groups from the converters 118 and 120 and outputs data blocks. The block buffer memory 130 also contains write and read address generators which control the writing and reading of data. Each data block contains at least one data group (e.g., 8 bits) and sequentially outputs the data blocks from each of the data demodulators and decoders 100 to the outer decoder 102 for sequential decoding as described below.

The processing of N BIT HARD DECISIONS requires only one data conversion of N BIT HARD DECISIONS from multiple channels which is performed by converter 120 while the processing performed by the N BIT SOFT DECISIONS from multiple channels requires sequential data conversions. The sequential data conversions are performed by the data demultiplexing and reordering memory 114 which packs two-bit symbols into bytes, which are decoded by the inner decoder 116 into an output nibble of the most likely bits from multiple TDM channels, which require further conversion by the nibble to byte converter 118 to output data words from multiple TDM channels of the correct length for decoding by the outer decoder 102.

The operation of the block buffer memory 130 is illustrated in FIG. 5 which represents processing of data encoded with the ATM protocol. As illustrated, the outputs from the R input channels produced by the individual data demodulator and decoders 100 are comprised of two hundred thirty-six bytes which are made up of four ATM cells each of fifty-three bytes and twenty-five parity bytes. The individual channel outputs containing four ATM cells including parity bits are written from all of the R channels in sequence into the block buffer memory 130. As illustrated, the inputs are written into storage in parallel and are outputted in serial blocks 1-R of two hundred thirty six bytes to the outer decoder.

The block buffer memory 130 functions to read out data at R times the individual X channel data input rate and functions in accordance with the relationship

$$AR = \left( \frac{SR}{Z} \right) \cdot R$$

wherein AR is the readout rate of the memory, SR is a symbol rate of data samples in the data groups, Z is a ratio of a length in bits of a block to a number of bits per symbol

and R is the number of parallel channels. This permits the outer decoder 102 to be designed to process the individual ATM frames each containing encoded multiple TDM channels of data of two hundred thirty six bytes sequentially so that the outer decoding function may be performed by the single outer decoder 102 for each of the R channels. This eliminates the need for multiple outer decoders 28 in the prior art of FIG. 1.

Substantially less hardware is required for the present invention as illustrated in FIG. 2 in comparison to the prior art of FIG. 1. This reduction in hardware is achieved by the combination of processing produced by the data demultiplexing and reordering memory 114, nibble to byte converter 118, dibit to byte converter 120 and block buffer memory 130. The data demultiplexing and reordering memory 114, nibble to byte converter 118 and dibit to byte converter 120 facilitate the necessary processing of multiple channels of TDM data to provide efficient multiple channel processing using common hardware instead of the single channel processing of the prior art which required a replication of processing hardware for each of the multiple channels. The high data access speed of the block buffer memory 130, is used to provide data at a high readout rate to the outer decoder 102 for decoding at a high data rate which may be greater than 28 megabytes per second when the individual input data rate to the block buffer 130 from the output of the individual data demodulators and decoders 100 is 4.67 megabytes per second for all of the X, Y and Z operational modes. A Reed-Solomon decoder, functioning as the outer decoder 102, has a pipeline processor architecture permitting the aforementioned sustained high throughput from multiple TDM channels.

While the invention has been described in terms of the preferred embodiment, it should be understood that numerous modifications may be made to the invention without departing from the spirit and scope of the invention. It is intended that all such modifications fall within the scope of the appended claims.

What is claimed is:

1. A receiver comprising:

a pair of data processing paths with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path;

first and second memories, connected in the soft decision processing path and the hard decision processing path, respectively, each memory including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal and outputs the stored data samples from a plurality of channels in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels;

wherein the soft decision processing path further comprises upstream of the first memory, another memory including an addressable storage array which stores a sequence of data samples contained in the time division multiplexed signal and outputs the stored data samples in a sequence of the data groups, each data group containing a plurality of samples from one of the plurality of channels and an inner decoder, responsive to the data groups, which decodes the data samples within the data groups and outputs the decoded data samples to the first memory in the soft decision processing path;

a block buffer memory coupled to receive data groups from a selected one of the soft decision processing path and the hard decision processing path; and

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- a single outer decoder coupled to receive data blocks of multichannel data from the block buffer memory, with each data block containing at least one data group, wherein the outer decoder decodes the data blocks and outputs decoded data blocks.
2. A receiver in accordance with claim 1 wherein: the data samples inputted to the another memory each comprise orthogonally encoded data; and the inner decoder is a biorthogonal decoder.
3. A receiver in accordance with claim 2 wherein: the inner decoder is a Reed-Muller decoder.
4. A receiver in accordance with claim 1 wherein: the receiver is contained in a satellite.
5. A receiver in accordance with claim 2 wherein: the receiver is contained in a satellite.
6. A receiver in accordance with claim 3 wherein: the receiver is contained in a satellite.
7. A receiver in accordance with claim 4 further comprising: a channelizer, which is responsive to an input bandwidth and divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the channels comprising the time division multiplexed signal.
8. A receiver in accordance with claim 1 wherein: each of the first and second memories further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator.
9. A receiver in accordance with claim 2 wherein: each of the first and second memories further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator; and the other memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the other memory with addresses generated by the write address generator and the sequence of data groups being read out from a group of memory cells of the other memory with addresses generated by the read address generator.
10. A receiver in accordance with claim 3 wherein: each of the first and second memories further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the

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- write address generator and the sequence of data groups being read out with addresses generated by the read address generator; and the other memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the other memory with addresses generated by the write address generator and the sequence of data groups being read out from a group of memory cells of the other memory with addresses generated by the read address generator.
11. A receiver in accordance with claim 4 wherein: each of the first and second memories further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator.
12. A method of data reception comprising: storing in first and second memories a received time division multiplexed signal containing a sequence of data samples from a plurality of channels; providing a pair of data processing paths with one of the data processing paths comprising a soft decision data processing path and another of the data processing paths comprising a hard decision data processing path, and wherein the hard decision data processing path and the soft decision processing path contain the first and second memories, respectively, each of the first and second memories storing a received time division multiplexed signal containing a sequence of data samples from the plurality of channels, wherein the soft decision path contains another memory, upstream of the second memory, which stores a sequence of the data samples and outputs the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels, and wherein each data group is decoded with an inner decoder, and wherein the decoded data decoded by the inner decoder is output to the second memory in the soft decision processing path; outputting from the first and second memories the stored data samples in a sequence of data groups with each data group containing a plurality of samples from one of the plurality of channels; inputting the sequence of data groups from the a selected one of the first and second memories into a block buffer memory; outputting data blocks of multichannel data into a single outer decoder, decoding with the outer decoder the data samples within data blocks with each data block containing at least one data group; and outputting the decoded data samples of the plurality of data blocks.
13. A method in accordance with claim 12 wherein: the data samples inputted to the another memory each comprise orthogonally encoded data; and the inner decoder is a biorthogonal data encoder.

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14. A method in accordance with claim 12 wherein:  
the method is performed within a satellite.

15. A method in accordance with claim 14 further comprising:

dividing an input bandwidth with a channelizer into a plurality of output channels each having an equal bandwidth, one of the output channels comprising the time division multiplexed signal.

16. A method in accordance with claim 12 further comprising:

addressing memory cells of each of the first and second memories by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

17. A method in accordance with claim 13 further comprising:

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addressing memory cells of each of the at least one memory by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

18. A method in accordance with claim 14 further comprising:

addressing memory cells of each of the first and second memories by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

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